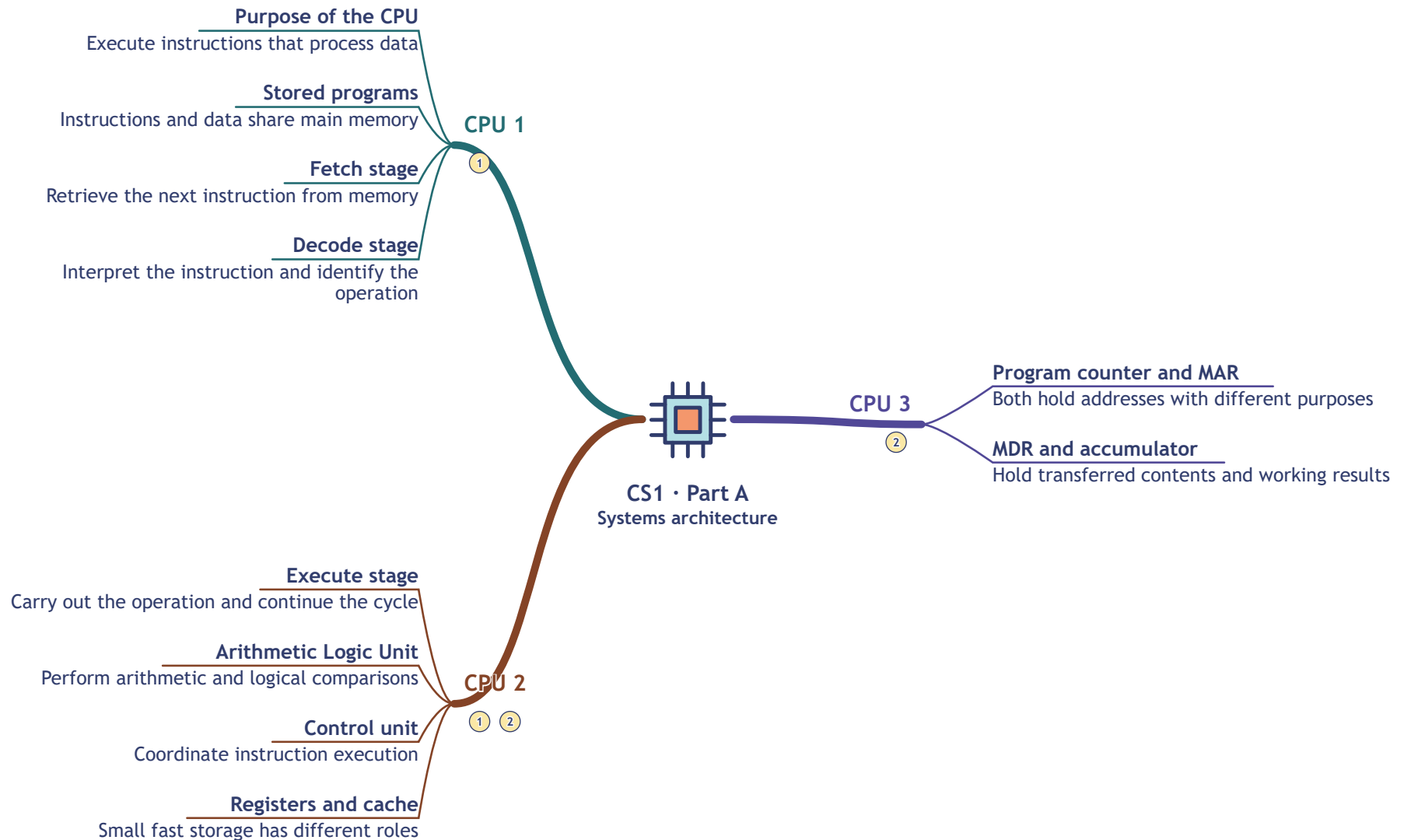




1. CPU 1 → CPU 2: Decoded instructions coordinate arithmetic and immediate working storage.
2. CPU 2 → CPU 3: Registers separately hold addresses, transferred contents and results.